Amendments to the Specification

A substitute specification (and an annotation thereof) that incorporates all changes after this current amendment is submitted herewith.

Please amend the specification as follows:

On page 2, Line 8, please replace the paragraph that begins "According to one aspect" with the following paragraph:

"According to one aspect of the invention, the chip comprises a monocrystalline silicon substrate layer whose active face has circuits integrated therein defining a central processor unit and memories. The chip further comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm. For example, an additional layer of monocrystalline silicon covers at least part of the active face."

On page 6, Line 4, please replace the paragraph that begins "In the first type as" with the following paragraph:

"In the first type as shown in Figure 3A, the chip 5 has a monocrystalline silicon substrate layer 12. This layer 12 has an active face 13 in which the circuits are integrated and a face opposite from said from said active face 13, i.e. the rear face 6. The contact pads 8 are generally five in number and they are integrated in the active face 13."

On page 6, Line 8, please replace the paragraph that begins "In a second type" with the following paragraph:

"In a second type of chip 5a shown in Figure 3B (and one variation thereof shown in Figure 4A), the chip 5a has in similar manner a monocrystalline silicon substrate layer 12a whose thickness has been reduced

and is therefore thinner than the monocrystalline silicon substrate layer 12 shown in Figure 3A. This monocrystalline silicon substrate layer 12a likewise has an active face 13a which includes the integrated circuits and a face opposite said active face, i.e. the rear face 6a."

On page 6, Line 14, please replace the paragraph that begins "However, the active face" with the following paragraph:

"However, the active face 13a is covered in an additional layer 14 of monocrystalline silicon which is ~~scaled~~bonded to said face 13a via a ~~scaling~~bonding layer 15. The additional layer 14 has a top face 18 and a bottom face 19 in contact with the ~~scaling~~bonding layer. The ~~scaling~~bonding layer 15 and the additional layer 14 advantageously cover all or at least a major portion of the active face 13a of chip 5a with the exception of the contact pads 8a which remain accessible through openings 16, or "vias", formed through said layers 14 and 15. In practice, the thickness of the various layers are as follows. Thinned substrate layer: about 15 μm; additional layer: about 150 μm; and ~~scaling~~bonding layer: about 10 μm."

On page 7, Line 19, please replace the paragraph that begins "Thus, the dopants" with the following paragraph:

"Thus, the dopants conventionally used for changing the semiconductive properties of monocrystalline silicon are capable of changing the absorption properties of an intrinsic crystal of silicon so that its absorption coefficient increases significantly at wavelengths longer than 1 μm, i.e. in particular, at wavelengths in the infrared range."

On page 8, Line 7, please replace the paragraph that begins "The dopants 17 can be incorporated" with the following paragraph:

"The dopants 17 can be incorporated in the crystal lattice while the monocrystalline silicon crystal is being grown, or else they can be the subject of high temperature diffusion under an inert atmosphere, or they can be the subject of ion implantation."

On page 8, Line 10, please replace the paragraph that begins "The dopants 17 can present" with the following paragraph:

"The dopants 17 can be present in the monocrystalline silicon substrate layer 12 of a chip 5 of the first type or of a chip 5a of the second type. They can also be incorporated in the additional layer 14 of a chip 5a of the second type."

On page 9, Line 3, please replace the paragraph that begins "In a second embodiment of the invention" with the following paragraph:

"In a second embodiment of the invention as shown in Figures 6A, 6B, 6C and 6D the means providing physical protection against the action of light are formed by surface irregularities 20 visible on a face of a layer of monocrystalline silicon. These surface irregularities can be visible on the rear face of the monocrystalline silicon substrate or on one or two of the top and bottom faces of the additional layer 14 for chips 5a of the second type."

On page 9, Line 11, please replace the paragraph that begins "In practice, the irregularities" with the following paragraph:

"In practice, the irregularities 20 are formed by etching the monocrystalline silicon, e.g. by means of a dry technique such as mechanical abrasion, or a wet technique such as potassium hydroxide (KOH) machining."

On page 9, Line 20, please replace the paragraph that begins "In the variant of Figure 6A" with the following paragraph:

"In the variant of Figure 6A which shows a chip 5a of the second type, the irregularities 20 are formed on the face of the additional layer 14 which comes into contact with the ~~scaling~~bonding layer 15."

On page 10, Line 1, please replace the paragraph that begins "In the variant of Figure 6B" with the following paragraph:

"In the variant of Figure 6B which shows a chip 5 of the first type, the irregularities 20 are formed in the rear face of the monocrystalline silicon substrate layer."

On page 10, Line 8, please replace the paragraph that begins "In a third embodiment of the invention shown" with the following paragraph:

"In a third embodiment of the invention shown in Figures 7A, 7B, 7C and 7D the physical protection means are formed by a metal layer 21 assembled on at least one of the faces of the substrate or additional layers 12 or 14 of monocrystalline silicon having a thickness of more than 50 Ångstroms (Å), e.g. about 100 Å."

On page 10, Line 19, please replace the paragraph that begins "In a third embodiment of the invention shown" with the following paragraph:

"In the variant of Figure 7A which shows a chip of the second type, the metal layer 21 is placed between the additional layer 14 and the ~~scaling~~bonding layer 15."

On page 11, Line 3, please replace the paragraph that begins "In the variant of Figure 7D" with the following paragraph:

"In the variant of Figure 7D which shows a chip 5a of the second type, a first metal layer is placed between the additional layer 14 and the ~~scaling~~bonding layer 15, and a second metal layer is placed on the rear face of the substrate layer 12a."